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|---|---|
| **Unit / Module Name:** | CameraLink Receiver Module |
| **Unit / Module Number:** | AV949 |
| **Used On:** | AV800 |
| **Document Issue:** | 1.1 |
| **Date:** | 12th March 2010 |

# CONFIDENTIAL

| Approvals | | Date |
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# Revision History

| Issue | Changes Made | Date | Initials |
|---|---|---|---|
| 0.9 | Initial Draft | 01/03/06 | AJP |
| 0.91 | Rename to AV949 | 21/03/07 | AJP |
| 0.95 | Description | 10/08/07 | AJP |
| 0.96 | Further Draft | 03/09/07 | AJP |
| 1.0 | Final Corrections | 06/09/07 | AJP |
| 1.1 | Template & Address Change | 12/03/2010 | AH |

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# 1 Introduction

The AV949 is a Camera Link interface, AVXB expansion card. Its can be attached to DSP modules such as the AV800 to allow interfacing of Camera Link devices.

The AV949 provides a Base, Medium and Full configuration Camera Link Interfaces through 2x 3M MDR connector. The interface also implements two serial interfaces between the card and the camera (one to the camera, one from the camera) as well as the four control lines to the camera.

When using base camera Links is it possible to configure the second connector as a second Base Camera Link input. Thus allowing the provision for attaching two cameras simultaneously. The AV949 uses 3 DS90CR288A LVDS decoders. These can each have a data rate output of up to 85MHz. Using the full capacity of 3 links data rates of upto 765 Mbytes per second can be achieved.

The module uses the Advanced Vision Expansion Bus (AVXB) in single ended mode in order to interface to DSP modules such as the AV800.

## 1.1 Related Documents

Advanced Vision Expansion Bus (AVXB) – AVT.

AV800 – Advanced Video Processing DSP Module.

# 2 Functional Description

Base Camera Link mode uses one Camera Link connectors and one of the Decoder IC's. The 24bit Data is fed with syncs and clocks to a LVTTL to 2.5V level converter before being fed to the AVXB connector. The Medium and Full Camera Link modes use the remaining connector and IC's in order to provide 2 and 3 times the data widths respectively.

The maximum permitted data clock for the interface is 85Mhz therefore allowing a theoretical maximum throughput of 765 M Bytes/Second.

## 2.1 CameraLink Receiver

The receiver is based on the DS90CR288A. These devices convert the four LVDS data streams back into 28 bits of LVCMOS/LVTTL data per device. For single link operation only one of these devices is used. When Medium CameraLink is used both connectors and 2 DS90CR288A are utilised. In Full CameraLink mode both connectors and all 3 receivers are used. The table in Figure 1 summarises the different modes the AV949 is capable of.

| Configuration | Ports | Supported Number of Chips | Number of Connectors |
|---|---|---|---|
| Base | A, B, C | 1 | 1 |
| Medium | A, B, C, D, E, F | 2 | 2 |
| Full | A, B, C, D, E, F, G, H | 3 | 2 |

**Figure 1 :Port Assignments According to Configuration**

A port is defined as an 8-bit word. The Least Significant Bit (LSB) is bit 0, and the Most significant Bit (MSB) is bit 7. The Camera Link interface utilizes the 8 ports of A-H.

## 2.2 AVXB Header

The Advanced Vision Expansion Bus (AVXB) allows data from each video decoder to be streamed, using embedded or separate sync formats, to the main processing module. All signals are LVPECL at 2.5V.

### 2.2.1 AVXB Power Supplies

When using the AVXB interface a separate AVXB power header (BKT) is used to supply the Daughterboard. Details of this connector pinout can be found in the AVXB Reference Guide.

## 2.3 Block Diagram

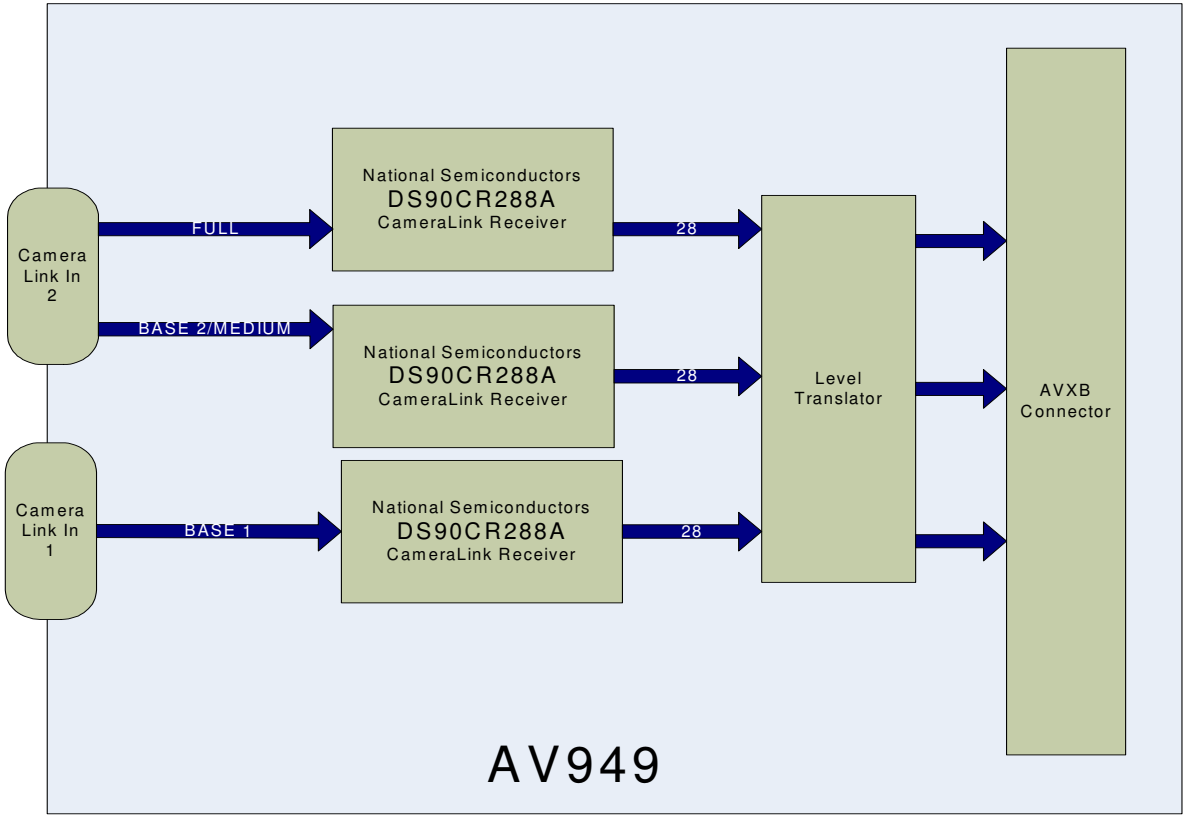
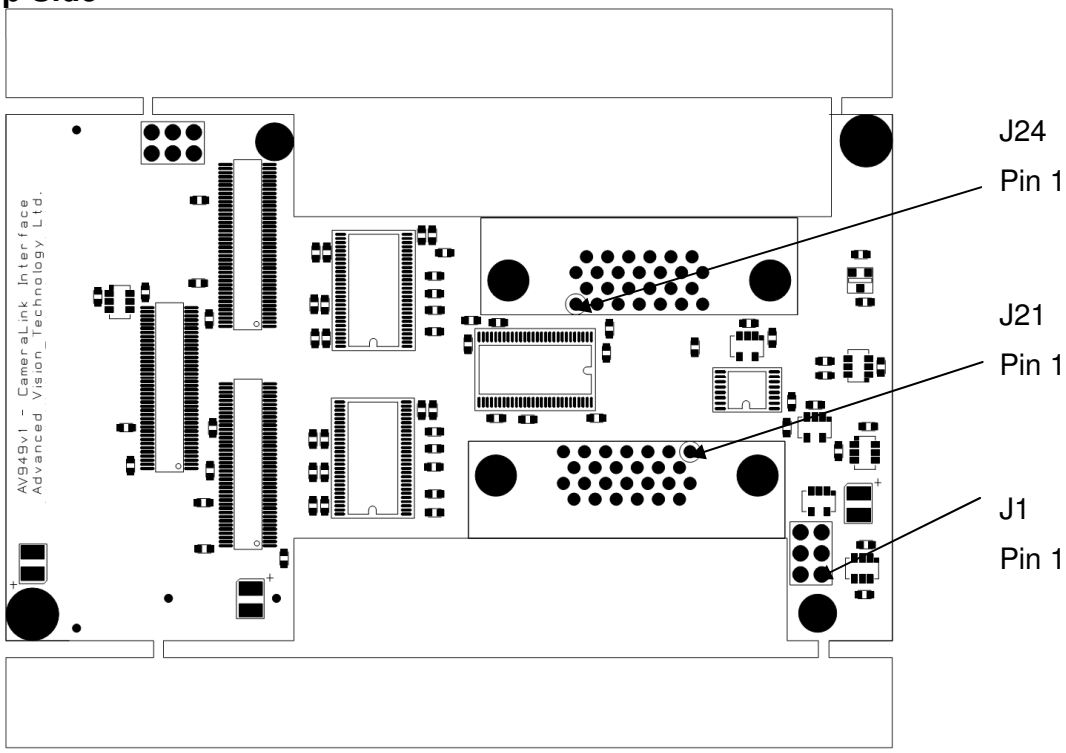



**Figure 2 : AV949 Block Diagram**

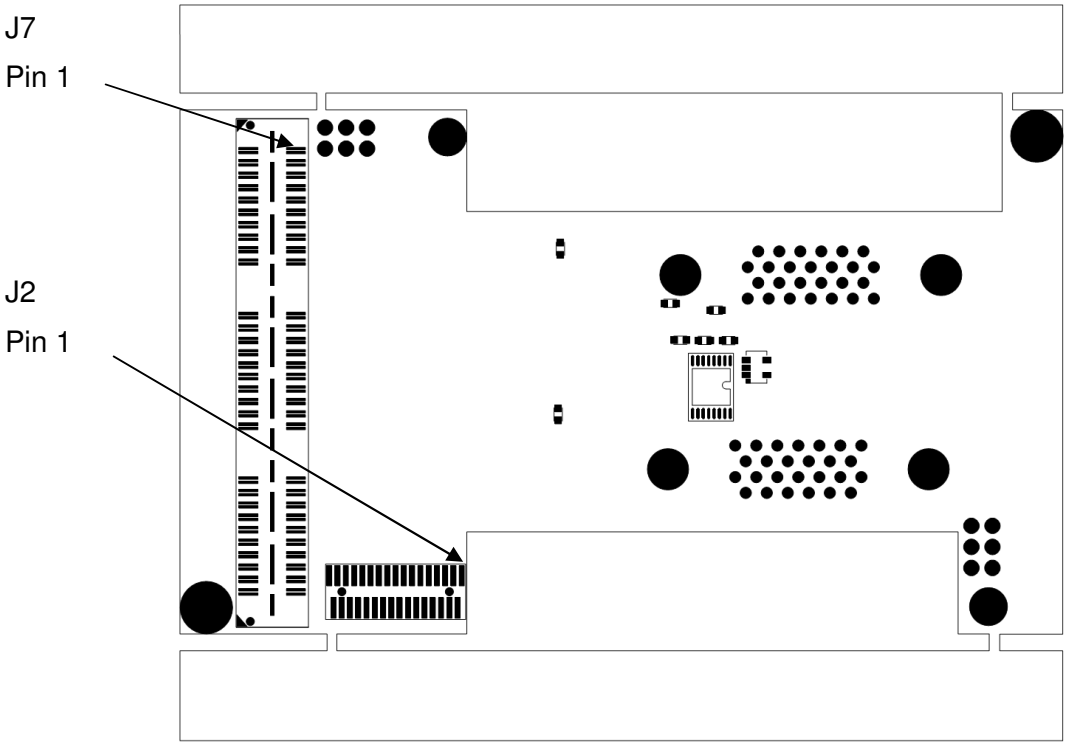
# 3 Mechanical Interface

The host board provides power, Ground, data and control lines between the module.

## 3.1 Top Side




## 3.2 Bottom Side



# 4 Electrical Interface

For pinout and information of the AVXB signal and power connectors see :

Advanced Vision Expansion Bus (AVXB) Specifications – AVT.

## 4.1 Camera Link Connector (J3)

AV949 Connector Part No. 3M N10226-5212PC

Mating Connector Part No. 3M 10126-6000EC

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Inner Shield | 14 | Inner Shield |
| 2 | CAM_CTRL4+ | 15 | CAM_CTRL4- |
| 3 | CAM_CTRL3+ | 16 | CAM_CTRL3- |
| 4 | CAM_CTRL2+ | 17 | CAM_CTRL2- |
| 5 | CAM_CTRL1+ | 18 | CAM_CTRL1- |
| 6 | Ser_TFG+ | 19 | Ser_TFG- |
| 7 | Ser_TC- | 20 | Ser_TC+ |
| 8 | CAM_X3+ | 21 | CAM_X3- |
| 9 | CAM_CLKX+ | 22 | CAM_CLKX- |
| 10 | CAM_X2+ | 23 | CAM_X0- |
| 11 | CAM_X1+ | 24 | CAM_X1- |
| 12 | CAM_X0+ | 25 | CAM_X0- |
| 13 | Inner Shield | 26 | Inner Shield |

## 4.2 Camera Link Connector (J4)

AV949 Connector Part No. 3M N10226-5212PC

Mating Connector Part No. 3M 10126-6000EC

| Pin | Signal Base2 / MediumFull | Pin | SignalBase2 / MediumFull |
|---|---|---|---|
| 1 | Inner Shield | 14 | Inner Shield |
| 2 | CAM_CTRL2_4+/ CAM_Z3+ | 15 | CAM_CTRL2_4-/ CAM_Z3- |
| 3 | CAM_CTRL2_3+/ CAM_Z2+ | 16 | CAM_CTRL2_3-/ CAM_Z2- |
| 4 | CAM_CTRL2_2+/ CAM_Z1+ | 17 | CAM_CTRL2_2-/ CAM_Z1- |
| 5 | CAM_CTRL2_1+/ CAM_Z0+ | 18 | CAM_CTRL2_1-/ CAM_Z0- |
| 6 | Ser_TFG2+ | 19 | Ser_TFG2- |
| 7 | Ser_TC2- | 20 | Ser_TC2+ |
| 8 | CAM_X3+/ CAM_Y3+ | 21 | CAM_X3-/ CAM_Y3- |
| 9 | CAM_CLKX+/ CAM_CLKY+ | 22 | CAM_CLKX- / CAM_CLKY- |
| 10 | CAM_X2+/ CAM_Y2+ | 23 | CAM_X0- / CAM_Y2- |
| 11 | CAM_X1+ CAM_Y1+ | 24 | CAM_X1- / CAM_Y1- |
| 12 | CAM_X0+ / CAM_Y0+ | 25 | CAM_X0- / CAM_Y0- |
| 13 | Inner Shield | 26 | Inner Shield |

## 4.3 AVXB Interface Connector(J7)

AV949 Connector Part No. Samtec QSH-060-01-F-D-DP-A

Mating Cable Part No. Samtec HFHM2-060-T-5.00-DP

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|---|---|---|---|---|---|---|---|
| 1 | CAMERA PF5 | 2 | CAMERA PG0 | 3 | CAMERA_B2_LVAL | 4 | CAMERA PG1 |
| 5 | CAMERA B2_FVAL | 6 | CAMERA PG2 | 7 | CAMERA B2_DVAL | 8 | CAMERA PG3 |
| 9 | CAMERA PD6 | 10 | CAMERA PG4 | 11 | CAMERA PF4 | 12 | CAMERA PG5 |
| 13 | CAMERA PF3 | 14 | CAMERA PG6 | 15 | CAMERA PF2 | 16 | CAMERA PG7 |
| 17 | CAMERA PF1 | 18 | | 19 | CAMERA PF7 | 20 | |
| 21 | CAMERA PF0 | 22 | CAMERA PF6 | 23 | CAMERA PE5 | 24 | CAMERA PE4 |
| 25 | CAMERA PE7 | 26 | CAMERA PE3 | 27 | CAMERA PE6 | 28 | CAMERA PE2 |
| 29 | CAMERA PE0 | 30 | CAMERA PE1 | 31 | CAMERA PD5 | 32 | CAMERA PD7 |
| 33 | CAMERA PD3 | 34 | CAMERA PD4 | 35 | CAMERA PD0 | 36 | CAMERA PD1 |
| 37 | | 38 | | 39 | CAMERA 2 SerTC | 40 | CAMER 2 SerTFG |
| 41 | | 42 | CAMERA 2 CLK | 45 | | 44 | |
| 45 | CAMERA CTL1 | 46 | CAMERA CTL2 | 47 | CAMERA CTL3 | 48 | CAMERA CTL4 |
| 49 | | 50 | | 51 | | 52 | |
| 53 | | 54 | | 55 | CAMERA 1 CLK | 56 | |
| 57 | | 58 | | 59 | | 60 | |
| 61 | | 62 | | 63 | | 64 | |
| 65 | CAMERA 2 CTL1 | 66 | CAMERA 2 CTL4 | 67 | CAMERA 2 CTL2 | 68 | |
| 69 | CAMERA 2 CTL3 | 70 | | 71 | | 72 | |
| 73 | | 74 | | 75 | | 76 | |
| 77 | | 78 | | 79 | | 80 | |
| 81 | CAMERA PC5 | 82 | CAMERA PH0 | 83 | CAMERA LVAL | 84 | CAMERA PH1 |
| 85 | CAMERA FVAL | 86 | CAMERA PH2 | 87 | CAMERA DVAL | 88 | CAMERA PH3 |
| 89 | CAMERA PA6 | 90 | CAMERA PH4 | 91 | CAMERA PC4 | 92 | CAMERA PH5 |
| 93 | CAMERA PC3 | 94 | CAMERA PH6 | 95 | CAMERA PC2 | 96 | CAMERA PH7 |
| 97 | CAMERA PC1 | 98 | | 99 | CAMERA PC7 | 100 | |
| 101 | CAMERA PC0 | 102 | CAMERA PC6 | 103 | CAMERA PB5 | 104 | CAMERA PB4 |
| 105 | CAMERA PB7 | 106 | CAMERA PB3 | 107 | CAMERA PB6 | 108 | CAMERA PB2 |
| 109 | CAMERA PB0 | 110 | CAMERA PB1 | 111 | CAMERA PA5 | 112 | CAMERA PA7 |
| 113 | CAMERA PA3 | 114 | CAMERA PA4 | 115 | CAMERA PA0 | 116 | CAMERA PA1 |
| 117 | CAMERA PA0 | 118 | CAMERA Clock | 119 | CAMERA SerTC | 120 | CAMER SerTFG |

## 4.4 JTAG Pass Through Connector (J1)

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | NA | 2 | NA |
| 3 | NA | 4 | NA |
| 5 | NA | 6 | NA |

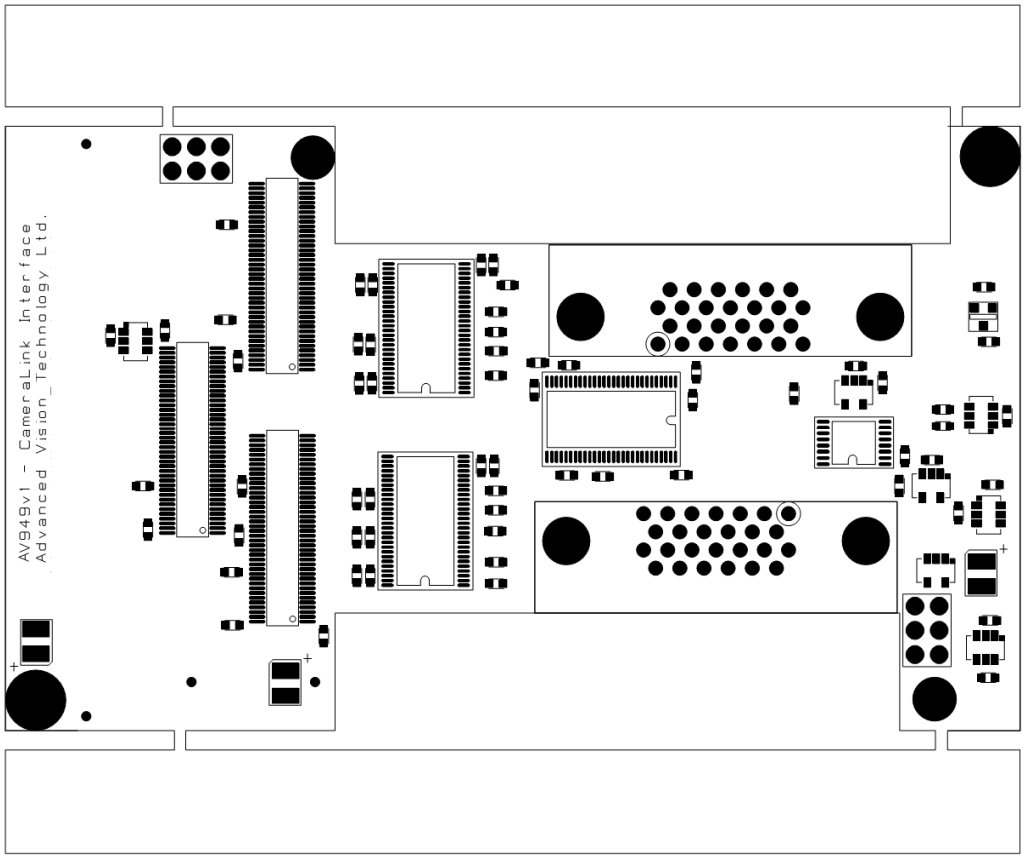
# 5 Verification Procedures

The verification procedure for the module is as follows.

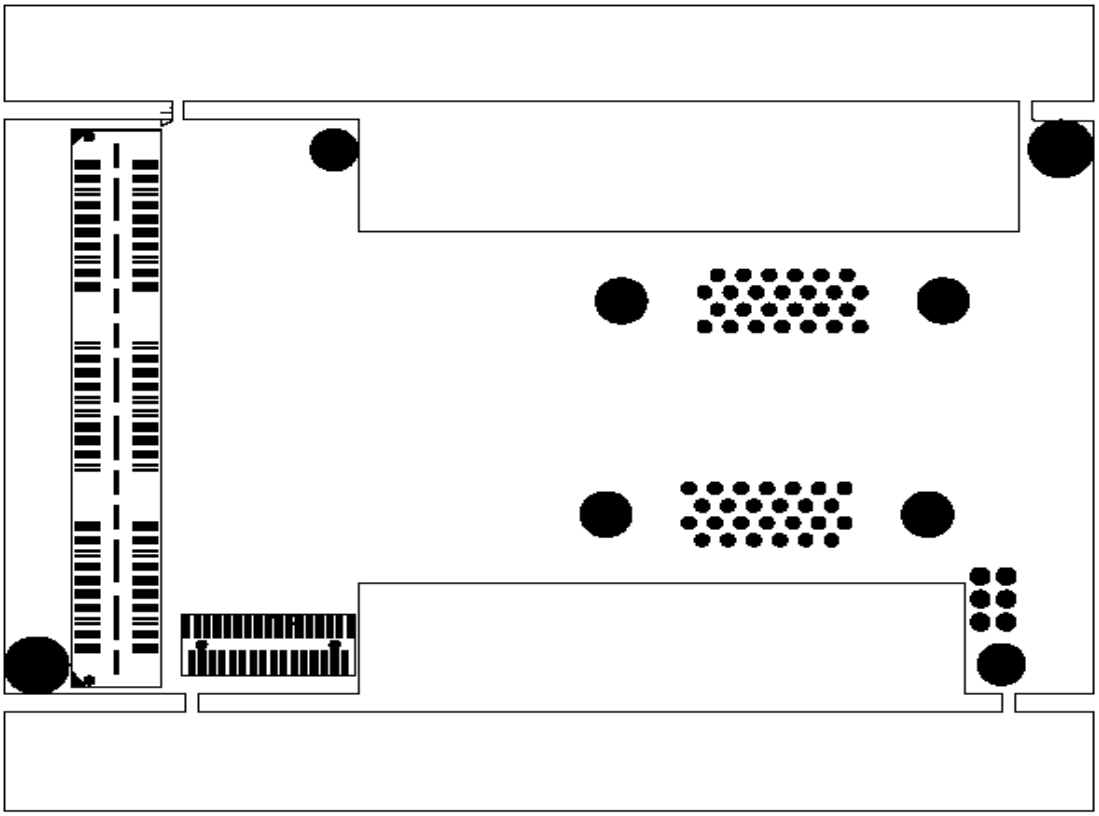
1. A Base configuration Camera is connected to Primary connector and the image is verified with a series of test patterns aquired with the camera.
2. The same Camera is connected to the Secondary connector and the Base 2 camera connection is validated as in 1.
3. The Camera control signals are validated using a simple test program lights up the control LED's on the AV949
4. The camera parameters are varied in both Base link positions to validate the 2 way communications

# 6 PCB Layout Details

## 6.1 Top Side




## 6.2 Bottom Side



# 7 Safety

This module presents no hazard to the user.

# 8 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system.

This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the output cables.

Short circuiting any output to ground does not cause the host PC system to lock up or reboot.